CUSTOMER NO.
48744

SPECIFICATION AMENDMENTS

Please amend the Specification as indicated:

Please replace paragraph **[0016]** with the following amended paragraph:

[0016] FIG. 5 illustrates a memory map of the computer system of FIG. 2; and

Please replace paragraph **[0021]** with the following amended paragraph:

[0021] In addition, Southbridge 140 has a bus known as a system management (SM) bus labeled "SM BUS" 160 by which it is connected to memory 134. SM BUS 160 is the mechanism by which CPU 110, under the control of the BIOS program stored in BIOS ROM 150, is able to perform memory tests on memory 134 at startup. This conventional memory test may be performed as follows. After CPU 110 comes up out of reset, it fetches a reset vector pointing to a location in BIOS ROM 150 containing the startup program sequence. One of the items performed in the startup program sequence is to determine the configuration of memory 134. The BIOS directs Southbridge 140 to poll memory 134 over SM bus 160 to determine how much memory is installed. After determining the memory configuration, the BIOS performs a memory check through Northbridge 120. For example, the BIOS may cause CPU 110 ~~may~~ to write a predefined test pattern (e.g., $55) to all memory locations, and subsequently read the memory locations to determine whether the test pattern was correctly stored. Later an opposite test pattern may be applied (e.g., $AA) to all memory locations and read back to determine whether each memory cell may assume either logic state. Any bad memory element is noted and used to configure Northbridge 120, and in this way, bad memory may be mapped out of the system.

Please replace paragraph **[0023]** with the following amended paragraph:

[0023] An alternate way of performing a memory test in a multiprocessor computer system can be better understood with reference to FIG. 2, which illustrates a block diagram of a multiprocessor computer system 200 according to the present invention. Computer system 200 includes generally eight processor nodes 210-217 connected in an array or fabric in which each node is connected to one or more adjacent nodes. For example, system [[100]] 200 is an eight-

processor system in which node 210 labeled "0" is connected to adjacent nodes 1 and 7; node 211 labeled "1" is connected to adjacent nodes 0, 2, and 5; and so on. Each node used in system 200 has three available link controllers which are connected to either adjacent processor nodes or to I/O devices. Since nodes 0, 2, 4 and 6 use only two of their available three link controllers to connect to adjacent processor nodes, they have an additional link controller available for connection to I/O devices.

Please replace paragraph **[0026]** with the following amended paragraph:

[0026] In order to determine the memory configuration in this multiprocessor system, one of the nodes is selected to be the boot strap processor (BSP). In system 200, node 210 is the BSP (referred to hereinafter as BSP 210), and it includes a link controller connected to an I/O device in the form of a Southbridge 250, which in turn is connected to a BIOS ROM 260. Note that as used herein "BIOS" [[can]] refers to either the software stored in BIOS ROM 260 or the device storing the software, as the context dictates. Note that the BIOS can be stored in any of a variety of known storage media, including an erasable programmable ROM (EPROM), and electrically erasable programmable ROM (EEPROM), a flash EEPROM, and the like..

Please replace paragraph **[0048]** with the following amended paragraph:

[0048] Routine 600 starts with NODE# = 0(in a step not shown in FIG. 6) and continues until it either finds the NODE# and CS# of the failing address, or has tested all the nodes without success. It detects whether [[al]] <u>all</u> the nodes have been tested by determining <u>whether</u> the current NODE# is equal to the number of TOTAL NODES at step 602. For example, system 200 includes eight nodes so TOTAL NODES is equal to 8. If routine 600 reaches step 602 with NODE# = 8 (having tested all eight nodes from NODE# = 0 through NODE# = 7), it exits at step 609 without having found an appropriate CS#.